**CLAIMS**:

1. A microelectronic device fabricating method comprising:

providing a substrate having at least one beveled portion;

forming a layer of structural material on at least the at least one beveled portion; and

removing at least a portion of the structural material from the at least one beveled portion by anisotropic etching to form a device feature from the structural material.

2. The method of claim 1, wherein the substrate comprises a layer of insulative material over a semiconductive wafer, the structural material being formed over the insulative material.

3. The method of claim 1, wherein the bevel is less than or equal to about 45°.

4. The method of claim 1, wherein the substrate comprises a raised mandril and a semiconductive wafer, the raised mandril being positioned over the wafer and having four edges, including two edges substantially perpendicular to the wafer and two beveled edges, the structural material being formed over at least one beveled edge.

5. The method of claim 1, wherein the forming of structural material comprises depositing a substantially uniformly thick layer of structural material over the substrate.

6. The method of claim 1, wherein the structural material comprises a chemical reaction or diffusion barrier material.

7. The method of claim 6, wherein the barrier material comprises a metal comprising oxide or metal comprising nitride.

8. The method of claim 1, wherein the removing of structural material comprises removing only a portion of the structural material from the at least one beveled portion to leave a pair of spaced, adjacent structural material lines on the at least one beveled portion.

9. The method of claim 1, wherein the device feature comprises a pair of spaced, adjacent, chemical reaction or diffusion barrier material lines which are substantially void of residual shorting stringers extending therebetween.

10. The method of claim 1, wherein the removing of structural material comprises removing substantially all of the structural material from the at least one beveled portion but leaving at least a portion of the structural material on another portion of the substrate.

11. The method of claim 10, wherein the structural material is conductive.

12. The method of claim 1, wherein the device feature comprises an edge defined feature.

13. A microelectronic device fabricating method comprising:

providing a substrate having at least one beveled portion;

forming a layer of structural material on the substrate, including on the at least one beveled portion; and

removing only a portion of the structural material from the at least one beveled portion by anisotropic etching to form a device feature from the structural material on the at least one beveled portion.

14. The method of claim 13, wherein the substrate comprises a layer of insulative material over a semiconductive wafer, the structural material being formed over the insulative material.

15. The method of claim 13, wherein the bevel is less than or equal to about 45°.

16. The method of claim 13, wherein the forming of structural material comprises depositing a substantially uniformly thick layer of structural material over the substrate.

17. The method of claim 13, wherein the structural material comprises a chemical reaction or diffusion barrier material.

18. The method of claim 13, wherein the device feature comprises a pair of spaced, adjacent lines on the at least one beveled portion.

19. The method of claim 13, wherein the device feature comprises a pair of spaced, adjacent, chemical reaction or diffusion barrier material lines which are substantially void of residual shorting stringers extending therebetween.

20. A microelectronic device fabricating method comprising:

providing a substrate having at least one beveled portion, wherein the bevel is less than or equal to about 45°;

forming a layer of chemical reaction or diffusion barrier material over the substrate, including over the at least one beveled portion;

forming a resist mask pattern over the barrier material; and

with the mask pattern in place, anisotropically etching to form a pair of spaced, adjacent barrier material lines which are substantially void of residual shorting stringers extending therebetween.

21. The method of claim 20, wherein the substrate comprises a layer of insulative material over a semiconductive wafer, the barrier material being formed over the insulative material.

22. The method of claim 20, wherein the forming of structural material comprises depositing a substantially uniformly thick layer of structural material over the substrate.

23. The method of claim 20, wherein the barrier material comprises a metal comprising oxide or metal comprising nitride.

24. A microelectronic device fabricating method comprising:

providing a substrate with a base surface and a raised surface, the raised surface being raised out from the base surface and having at least one edge substantially perpendicular to the base surface and at least one beveled edge;

forming a layer of structural material on at least the at least one perpendicular edge and the at least one beveled edge; and

removing an effective amount of the structural material from the at least one beveled edge, the base surface, and the raised surface while leaving an effective amount of the structural material on the perpendicular edge to form an edge defined feature from the structural material on at least the at least one perpendicular edge.

25. The method of claim 24, wherein the substrate comprises a layer of insulative material over a semiconductive wafer, the structural material being formed over the insulative material.

26. The method of claim 24, wherein the bevel is less than or equal to about 45°.

27. The method of claim 24, wherein the raised surface comprises a mandril and the base surface comprises a semiconductive wafer, the mandril being positioned over the wafer and having four edges, including two edges substantially perpendicular to the wafer and two beveled edges.

28. The method of claim 24, wherein the forming of structural material comprises depositing a substantially uniformly thick layer of structural material over the substrate.

29. The method of claim 24, wherein the removing of structural material comprises removing substantially all of the structural material from the at least one beveled edge but leaving at least a portion of the structural material on the at least one perpendicular edge of the substrate.

30. The method of claim 29, wherein the structural material is conductive.

31. The method of claim 24, wherein the device feature comprises an edge defined feature.

32. A microelectronic device fabricating method comprising:

providing a raised mandril over a substrate, the raised mandril being raised out from the substrate and having at least one edge substantially perpendicular to the substrate and at least one beveled edge;

forming a layer of conductive material on at least the at least one perpendicular edge and the at least one beveled edge;

anisotropically etching an effective amount of the conductive material from the at least one beveled edge, the substrate, and the mandril while leaving an effective amount of the conductive material on the perpendicular edge to form an edge defined feature from the conductive material on the at least one perpendicular edge; and

removing substantially all of the mandril.

33. The method of claim 32, wherein the substrate comprises a layer of insulative material over a semiconductive wafer, the conductive material being formed over the insulative material.

34. The method of claim 32, wherein the bevel is less than or equal to about 45°.

35. The method of claim 32, wherein the substrate comprises a semiconductive wafer, the raised mandril being positioned over the wafer and having four edges, including two edges substantially perpendicular to the wafer and two beveled edges.

36. The method of claim 32, wherein the forming of conductive material comprises depositing a substantially uniformly thick layer of conductive material over the substrate.

37. A microelectronic device fabricating method comprising:

forming a resist mask pattern on a substrate, the resist pattern having at least one beveled portion at an edge of at least one opening in the resist pattern;

transferring the resist pattern to the substrate to form at least one beveled portion of the substrate;

forming a layer of structural material on at least the at least one beveled portion of the substrate; and

removing at least a portion of the structural material from the at least one beveled portion by anisotropic etching to form a device feature from the structural material.

38. The method of claim 37, wherein the substrate comprises a layer of insulative material over a semiconductive wafer, the structural material being formed over the insulative material.

39. The method of claim 37, wherein the bevel is less than or equal to about 45°.

40. The method of claim 37, wherein the transferring the resist pattern forms a raised mandril from the substrate, the mandril having four edges, including two edges substantially perpendicular to a recessed portion of the substrate and two beveled edges, the structural material being formed over at least one beveled edge.

41. The method of claim 37, wherein the forming of structural material comprises depositing a substantially uniformly thick layer of structural material over the substrate.

42. The method of claim 37, wherein the structural material comprises a chemical reaction or diffusion barrier material.

43. The method of claim 42, wherein the barrier material comprises a metal comprising oxide or metal comprising nitride.

44. The method of claim 37, wherein the removing of structural material comprises removing only a portion of the structural material from the at least one beveled portion to leave a pair of spaced, adjacent structural material lines on the at least one beveled portion.

45. The method of claim 37, wherein the device feature comprises a pair of spaced, adjacent, chemical reaction or diffusion barrier material lines which are substantially void of residual shorting stringers extending therebetween.

46. The method of claim 37, wherein the removing of structural material comprises removing substantially all of the structural material from the at least one beveled portion but leaving at least a portion of the structural material on another portion of the substrate.

47. The method of claim 46, wherein the structural material is conductive.

48. The method of claim 37, wherein the device feature comprises an edge defined feature.

49. A microelectronic device fabricating method comprising:

providing a layer of resist material on a substrate;

exposing the resist to actinic energy providing gradated exposure of a second resist region;

developing the resist to remove a first region, revealing the substrate, and a portion of the second region, without revealing the substrate, while leaving a third region in place to form a resist mask pattern on the substrate, wherein a beveled portion of the resist pattern forms in the second region;

transferring the resist pattern to the substrate to form at least one beveled portion of the substrate;

forming a layer of structural material on at least the at least one beveled portion of the substrate; and

removing at least a portion of the structural material from the at least one beveled portion by anisotropic etching to form a device feature from the structural material.

50. The method of claim 49, wherein the substrate comprises a layer of insulative material over a semiconductive wafer, the structural material being formed over the insulative material.

51. The method of claim 49, wherein the bevel is less than or equal to about 45°.

52. The method of claim 49, wherein the transferring the resist pattern forms a raised mandril from the substrate, the mandril having four edges, including two edges substantially perpendicular to a recessed portion of the substrate and two beveled edges, the structural material being formed over at least one beveled edge.

53. The method of claim 49, wherein the forming of structural material comprises depositing a substantially uniformly thick layer of structural material over the substrate.

54. The method of claim 49, wherein the structural material comprises a chemical reaction or diffusion barrier material.

55. The method of claim 54, wherein the barrier material comprises a metal comprising oxide or metal comprising nitride.

56. The method of claim 49, wherein the removing of structural material comprises removing only a portion of the structural material from the at least one beveled portion to leave a pair of spaced, adjacent structural material lines on the at least one beveled portion.

57. The method of claim 49, wherein the device feature comprises a pair of spaced, adjacent, chemical reaction or diffusion barrier material lines which are substantially void of residual shorting stringers extending therebetween.

58. The method of claim 49, wherein the removing of structural material comprises removing substantially all of the structural material from the at least one beveled portion but leaving at least a portion of the structural material on another portion of the substrate.

59. The method of claim 58, wherein the structural material is conductive.

60. The method of claim 49, wherein the device feature comprises an edge defined feature.

61. An integrated circuit comprising:

a) a semiconductive substrate;

b) a layer of dielectric material over the substrate, the dielectric material layer having a base surface and a raised surface, the raised surface being raised out from the base surface and having at least one beveled edge and a step parallel to the base surface; and

c) a pair of spaced, adjacent, chemical reaction or diffusion barrier material lines with a portion extending over the at least one beveled edge from the base surface to the step of the raised surface, wherein the spaced lines are substantially void of residual shorting stringers extending therebetween.

62. The integrated circuit of claim 61, wherein the bevel is less than or equal to about 45°.

63. The integrated circuit of claim 61, wherein the barrier material comprises a metal comprising oxide or metal comprising nitride.

64. An intermediate construction of an integrated circuit comprising:

a) a semiconductive substrate;

b) a raised mandril over the substrate, the raised mandril being raised out from the substrate and having at least one edge substantially perpendicular to the substrate and at least one beveled edge; and

c) a layer of structural material forming an edge defined feature on the at least one perpendicular edge.

65. The method of claim 64, wherein the bevel is less than or equal to about 45°.

66. The method of claim 64, wherein the raised mandril comprises four edges, including two edges substantially perpendicular to the substrate and two beveled edges.

67. The method of claim 64, wherein the structural material is conductive.